What is claimed is:

1. A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:

a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry; and

reset means for resetting said plurality of flip-flops when transitioning from said normal operation mode to said test mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal.

2. The semiconductor integrated circuit according to Claim 1, wherein said reset means resets said plurality of flip-flops when transitioning from said test mode to said normal operation mode in accordance with said mode signal.

3. The semiconductor integrated circuit according to Claim 2, further comprising output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode.

4. The semiconductor integrated circuit according to Claim 3, further comprising:

memory means connected to said plurality of flip-flops; and

access control means for prohibiting access to said memory means during said test mode in accordance with said mode signal.

5. A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry,

comprising:

a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry;

reset means for resetting said plurality of flip-flops when transitioning from said test mode to said normal operation mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal.

6. The semiconductor integrated circuit according to Claim 1, further comprising transition detection means for detecting the transition timing of said logical level of said mode signal, wherein

said reset means resets said plurality of flip-flops when said transition timing detection means detects said transition timing.

7. The semiconductor integrated circuit according to Claim 5, further comprising transition detection means for detecting the transition timing of said logical level of said mode signal, wherein

said reset means resets said plurality of flip-flops when said transition timing detection means detects said transition timing.

8. A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:

a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry; and

output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode, while prohibiting the outputting of data that is supplied during said normal operation mode.

9. A semiconductor integrated circuit having a normal operation

mode and a test mode for scan testing internal logical circuitry, comprising:

a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry;

memory means connected to said plurality of flip-flops; and

access control means for prohibiting access to said memory means during said test mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal.

10. A method of testing a semiconductor integrated circuit, which has internal logical circuitry and a plurality of flip-flops for scan testing said internal logical circuitry, and which has a normal operation mode and a test mode for performing said scan testing, wherein

said plurality of flip-flops are reset when transitioning from said normal operation mode to said test mode.

11. A method of testing a semiconductor integrated circuit, which has internal logical circuitry and a plurality of flip-flops for scan testing said internal logical circuitry, and which has a normal operation mode and a test mode for performing said scan testing, wherein

said plurality of flip-flops are reset when transitioning from said test mode to said normal operation mode.

12. A method of testing a semiconductor integrated circuit, which has internal logical circuitry, a plurality of flip-flops for scan testing said internal logical circuitry and memory means connected to said plurality of flip-flops, and which has a normal operation mode and a test mode for performing said scan testing, wherein

access to said memory means is prohibited during said test mode.